What is claimed is:

1. A method for simulating an electric characteristic of a circuit including transistors, comprising the steps of:

arranging a plurality of transistors in a matrix pattern on the basis of sizes of the transistors, and storing data of the electric characteristic measured on first transistors among the plurality of transistors in the matrix pattern;

when a position of a second transistor different from the first transistors is specified in the matrix pattern, determining data of the electric characteristic of the second transistor according to interpolation rules by using the measured data of the one or more first transistors if there are one or more first transistors in the plurality of first transistor at one or more positions adjacent to the position of the second transistor in the matrix pattern; and

when a position of a third transistor different from the first and second transistors is specified in the matrix pattern, determining data of the electric characteristic of the third transistor according to the interpolation rules by using the measured data of the one or more first transistors and/or the interpolated data of the second transistor if there are one or more first transistors in the plurality of first transistor and/or one or more second transistor at one or more positions adjacent to the position of the third transistor in the matrix pattern.

2. The method as claimed in Claim 1, wherein the sizes of the plurality of transistors include gate length and gate width, the matrix pattern is a two-dimensional pattern of gate length and gate width, and the

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interpolation rules are defined on the basis of a function of the gate length and the gate width of the transistors.

3.   The method as claimed in Claim 1, wherein the interpolation rules are defined on the basis of a function of gate voltage of the plurality of transistors wherein threshold voltage thereof is taken into account.